IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1 and 16 in accordance with the following:

1. (CURRENTLY AMENDED) A parallel processor performing parallel processing of one or more basic instructions contained in each of a plurality of instruction words delimited by instruction delimiting information, said parallel processor comprising:

a plurality of instruction execution units performing processes in accordance with corresponding, supplied basic instructions in parallel;

an instruction fetch unit fetching the instruction words one by one in accordance with the instruction delimiting information; and

an instruction issue unit recognizing and, in accordance therewith, selectively issuing each of the basic instructions supplied from the instruction fetch unit to one of the corresponding instruction execution units to execute the issued basic instruction;

wherein the instruction issue unit comprises a conversion unit to generate an interface having effective bits ~~and instruction information~~ based on an~~the~~ instruction word~~s~~ format, the effective bits indicating availability of the corresponding instruction execution units and the instruction ~~information indicating a type of the corresponding instruction execution units~~word format indicating an arrangement of the basic instructions.

2. (ORIGINAL) The parallel processor as claimed in claim 1, wherein the plurality of instruction execution units all have the same structure.

3. (ORIGINAL) The parallel processor as claimed in claim 1, wherein:

at least two of the instruction execution units have different structures from each other; and

the instruction fetch unit rearranges the basic instructions contained in each of the fetched instruction words, in accordance with arrangement of the plurality of instruction execution units, and then supplies the rearranged basic instructions to the instruction issue unit.

4. (ORIGINAL) The parallel processor as claimed in claim 1, wherein:

at least two of the instruction execution units have different structures from each other; and

the instruction issue unit rearranges the basic instructions contained in each of the instruction words supplied from the instruction fetch unit, in accordance with arrangement of the plurality of instruction execution units, and then supplies the rearranged basic instructions to the instruction execution units.

5. (ORIGINAL) The parallel processor as claimed in claim 1, wherein:

at least two of the instruction execution units have different structures from each other;

the instruction fetch unit rearranges the basic instructions contained in each of the fetched instruction words, in accordance with arrangement of the instruction execution units, and then supplies the rearranged basic instructions to the instruction issue unit; and

the instruction issue unit further rearranges the basic instructions contained in each of the instruction word supplied from the instruction fetch unit, in accordance with the arrangement of the instruction execution units, and then supplies the rearranged basic instructions to the instruction execution units.

6. (ORIGINAL) The parallel processor as claimed in claim 3, wherein:

at least two of the instruction execution units have different structures from each other; and

the instruction fetch unit fetches an instruction word that contains basic instruction arranged in advance in accordance with the arrangement of the instruction execution units.

7. (PREVIOUSLY PRESENTED) The parallel processor as claimed in claim 1, wherein, depending on the type of a basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues a next basic instruction before the execution of the basic instruction being currently executed is completed.

8. (ORIGINAL) The parallel processor as claimed in claim 7, wherein, if a supplied basic instruction does not have data dependency or control dependency, or does not share resources with a basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues the supplied basic instruction before the execution of the basic instruction being currently executed is completed.

9. (CANCELLED) The parallel processor as claimed in claim 1, wherein the instruction issue unit further comprises an interface corresponding to the instruction execution units indicating whether the corresponding instruction execution unit is available.

10. (CANCELLED) A parallel processor as claimed in claim 9, wherein the instruction issue unit further comprises a table for setting effective bits to indicate availability of the corresponding instruction execution unit.

11. (PREVIOUSLY PRESENTED) A parallel processor as claimed in claim 1, wherein a first instruction word format is converted into a second instruction word format, the first instruction word format indicating a first arrangement of instruction words from the instruction fetch unit, and the second instruction word format indicating a second arrangement of instruction words which corresponds to the instruction execution units.

12. (PREVIOUSLY PRESENTED) A parallel processor as claimed in claim 1, wherein the conversion unit converts a first instruction word format into a second instruction word format on the basis of the effective bit, corresponding to the instruction execution units, indicating whether the corresponding instruction execution unit is available.

13. (PREVIOUSLY PRESENTED) A parallel processor as claimed in claim 12, wherein the first instruction word format indicates a first arrangement of instruction words from the instruction fetch unit, and the second instruction word format indicates a second arrangement of instruction words which corresponds to the instruction execution units.

14. (CANCELLED) A parallel processor performing parallel processing of one or more basic instructions contained in each of a plurality of instruction words delimited by instruction delimiting information, said parallel processor comprising:

an instruction issue unit recognizing and, in accordance therewith, selectively issuing each of the basic instructions to a corresponding instruction execution unit to execute the issued basic instruction.

15. (PREVIOUSLY PRESENTED) A parallel processor as claimed in claim 1, wherein the instruction issue unit issues the basic instructions to the corresponding instruction execution

unit based on the interface.

16. (CURRENTLY AMENDED) A parallel processor performing parallel processing of one or more basic instructions contained in each of a plurality of instruction words delimited by instruction delimiting information, said parallel processor comprising:

a plurality of instruction execution units performing processes in accordance with corresponding, supplied basic instructions in parallel;

an instruction fetch unit fetching the instruction words one by one in accordance with the instruction delimiting information;

an interface having effective bits corresponding to the instruction execution units, the effective bits indicating the corresponding instruction execution unit for each instruction word;

wherein the instruction words fetched by the instruction fetch unit have no attached dispersal information, and the effective bits are based on an instruction word format indicating an arrangement of the basic instructions.